Table 1

Address	Name	Default	RD/WR	Size	Comments
0x8000.0000	PADR	0	RW	8	Port A data register
0x8000.0001	PBDR	0	RW	8	Port B data
0x8000.0002	-		-	8	Reserved
0x8000.0003	PDDR	0	RW	8	Port D data
0x8000.0040	PADDR	0	RW	8	Port A data direction register
0x8000.0041	PBDDR	0	RW	8	Port B data
0x8000.0042	-		-	8	Reserved
0x8000.0043	PDDDR	0	RW	8	Port D data direction register
0x8000.0080	PEDR	0	RW	3	Port E data
0x8000.00C0	PEDDR	0	RW	3	Port E data
0x8000.0100	SYSCON	0	RW	32	System
0x8000.0140	SYSFLG	0	RD	32	System status flags register 1
0x8000.0180	MEMCFG 1	0	RW	32	Expansion and ROM memory configuration register 1
0x8000.01C0	MEMCFG 2	0	RW	32	Expansion and ROM memory
0x8000.0200	DRFPR	0	RW	8	DRAM refresh period register
0x8000.0240	INSTR1	0	RD	32	Interrupt status register 1

Address	Name	Default	RD/WR	Size	Comments
0x8000.0280	INTMR1	0	RW	32	Interrupt mask register 1
0x8000.02C0	LCDCON	0	RW	32	LCD control
0x8000.0300	TC1D	0	RW	16	Read/Write
0x8000.0340	TC2D	0	RW	16	Read/Write
0x8000.0380	RTCDR	-	RW	32	Realtime clock data register
0x8000.03C0	RTCMR	-	RW	32	Realtime clock match register
0x8000.0400	PMPCON	0	RW	12	PWM pump control register
0x8000.0440	CODR	0	RW	8	CODEC data I/O register
0x8000.0480	UARTDR 1	0	RW	8W/11 R	UART1 FIFO data register
0x8000.04C0	UBLCR1	0	RW	32	UART 1 bit rate and line
0x8000.0500	SYNCIO	0	RW	32	Synchronous serial I/O data register for master only SSI
0x8000.0540	PALMSW	0	RW	32	Least significant 32-bit word of LCD palette register

Address	Name	Default	RD/WR	Size	Comments
0x8000.0580	PALMSW	0	RW	32	Most significant 32-bit word of LCD palette register
0x8000.05C0	STFCLR	-	WR	-	Write to clear all start up reason flags
0x8000.0600	BLEOI	-	WR	-	Write to clear battery low interrupt
0x8000.0640	MCEOI	-	WR	-	Write to clear media changed interrupt
0x8000.0680	TEOI	-	WR	-	Write to clear tick
0x8000.06C0	TC1EOI	-	WR	-	Write to clear TC1 interrupt
0x8000.0700	TC2EOI	-	WR	-	Write to clear TC2 interrupt
0x8000.0740	RTCEOI	-	WR	-	Write to clear RTC match interrupt
0x8000.0780	UMSEOI	-	WR	-	Write to clear UART modem status changed interrupt
0x8000.07C0	COEOI	-	WR	-	Write to clear CODEC sound interrupt

Address	Name	Default	RD/WR	Size	Comments
0x8000.0800	HALT	-	WR	-	Write to enter the Idle State
0x8000.0840	STDBY	-	WR	-	Write to
0x8000.0880 0x8000.0FFF	Reserved				Write will have no effect, read is undefined
0x8000.1000	FBADDR	C	RW	4	LCD frame buffer start address
0x8000.1100	SYSCON2	0	RW	16	System control register 2
0x8000.1140	SYSFLG2	0	RD	16	System status register 2
0x8000.1240	INSTR2	0	RD	24	Interrupt status register 2
0x8000.1280	INTMR2	0	RW	16	Interrupt mask register 2
0x8000.12C0 - 0x80000.147F	Reserved				Write will have no effect, read is undefined
0x8000.1480	UARTDR2	0	RW	8W/11R	UART2 Data Register
0x8000.14C0	UBLCR2	0	RW	32	UART2 bit rate and line control register
0x8000.1500	SS2DR	0	RW	16	Master/slave SSI2 data Register

Address	Name	Default	RD/WR	Size	Comments
0x8000.1600	SRXEOF	-	WR	-	Write to clear RX FIFO overflow flag
0x8000.16C0	SS2POP	-	WR	-	Write to pop SSI2 residual byte into RX FIFO
0x8000.1700	KBDEOI	-	WR	-	Write to clear keyboard interrupt
0x8000.1800	Reserved	-	WR	-	Do not write to this location. A write will cause the processor to go into an unsupported power savings state.
0x8000.1840 - 0x8000.1FFF	Reserved	-			Write will have no effect, read is undefined

Table 2A

Interrupt	Bit in INTMR1 and INTSR1	Name	Comment
FIQ	0	EXTFIQ	External fast interrupt input (NEXTFIQ pin)
FIQ	1	BLINT	Battery low interrupt
FIQ	2	WEINT	Watchdog expired interrupt
FIQ	3	MCINT	Media changed interrupt

Interrupt	Bit in INTMR1 and INTSR1	Name	Comment
IRQ	4	CSINT	Codec sound interrupt
IRQ	5	EINT1	External interrupt input 1 (NEINT1 pin)
IRQ	6	EINT2	External interrupt input 2 (NEINT2 pin)
IRQ	7	EINT3	External interrupt input 3 (EINT3 pin)
IRQ	8	TC10I	TC1 underflow interrupt
IRQ	9	TC20I	TC2 undreflow interupt
IRQ	10	RTCMI	RTC compare match interrupt
IRQ	11	TINT	64 Hz tick interrupt
IRQ	12	UTXINT1	Internal UART 1 transmit FIFO empty interrupt
IRQ	13	URXINT1	Internal UART1 receive FIFO full interrupt
IRQ	14	UMSINT	Internal UART1 modem status changed interrupt
IRQ	15	SSEOTI	Synchronous serial interface 1 end of transfer interrupt

Table 2B

Interrupt	Bit in INTMR2 and INTSR2	Name	Comment
IRQ	0	KBDINT	Key press interrupt

Interrupt	Bit in INTMR2 and INTSR2	Name	Comment
IRQ	1	SS2RX	Master/slave SSI 16 bytes received
IRQ	2	SS2TX	Master/slave SSI 16 bytes transmitted
IRQ	12	UTXINT2	UART2 transmit FIFO empty interrupt
IRQ	13	URXINT2	UART2 receive FIFO full interrupt

TABLE 2C

Interrupt	Bit in INTMR3 and INTSR3	Name	Comment
FIQ	0	MCPINT	MCP interface interrupt

TABLE 3

Interrupt Pin	Input State	Operating State Latency	Idle State Latency	Standby State Latency
NEXTFIQ	Not deglitched; must be active for 20 μs to be detected	Worst case latency of 20 μs	Worst case 20 μs; if only single cycle instructions, less that 1 μs	Including PLL/ocs. setting time, approx. 0.25 s when FASTWAKE= 0, or approx. 500 μs when FASTWAKE = 1, or = Idle State if in 13 MHz mode with CLENSL set

Interrupt Pin	**Input State**	**Operating State Latency**	**Idle State Latency**	**Standby State Latency**
NEINT1-2	not deglitched	Worst case latency of 20 μs	As above	As above
EINT3	Not deglitched	Worst case latency of 20 μs	As above	As above
MEDCHG	Deglitched by 16 kHz clock; must be active for at least 80 μs to be detected	Worst case latenncy of 80 μs	Worst case 80 μs; if only single cycle instructions 61 μs	As above (note difference if in 13 MHz mode with CLKENSL set)

TABLE 4

PE[1]	PE[[0]	Boot Block (NCS0)
0	0	32-bit
0	1	8-bit
1	0	16-bit
1	1	Undefined

TABLE 5A

Address Range	Chip Select
0000.0000-0FFF.FFFF	CS7 (Internal only)
1000.0000-1FFF.FFFF	CS6 (Internal only)
2000.0000-2FFF.FFFF	NCS5
3000.0000-3FFF.FFFF	NCS4
4000.0000-4FFF.FFFF	NCS3
5000.0000-5FFF.FFFF	NCS2
6000.0000-6FFF.FFFF	NCS1
7000.0000-7FFF.FFFF	NCS0

TABLE 5B

Address Range	Chip Select
0000.0000-0FFF.FFFF	NCS0
1000.0000-1FFF.FFFF	NCS1
2000.0000-2FFF.FFFF	NCS2
3000.0000-3FFF.FFFF	NCS3
4000.0000-4FFF.FFFF	NCS4
5000.0000-5FFF.FFFF	NCS5
6000.0000-6FFF.FFFF	CS 6 (Internal only)
7000.0000-7FFF.FFFF	CS7 (Internal only)

TABLE 6

DRAM Address Pins	DRAM Column x16 Mode	DRAM Column x32 Mode	DRAM Row x 16§ Mode	DRAM Row x32 Mode	Pin Name
0	A1*	A2	A9	A10	A[27]/DRA[0]
1	A2	A3	A10	A11	A[26]/DRA[1]
2	A3	A4	A11	A12	A[25]/DRA[2]
3	A4	A5	A12	A13	A[24]/DRA[3]
4	A5	A6	A13	A14	A[23]/DRA[4]
5	A6	A7	A14	A15	A[22]/DRA[5]
6	A7	A8	A15	A16	A[21]/DRA[6]
7	A8	A9	A16	A17	A[20]/DRA[7]
8	A18	A19	A17	A18	A[19]/DRA[8]
9	A20	A21	A19	A20	A[18]/DRA[9]
10	A22	A23	A21	A22	A[17]/DRA[10]
11	A24	A25	A23	A24	A[16]/DRA[11]
12	A26	A27	A25	A26	A[15]/DRA[12]

TABLE 7

Size	Address Configuration	Total Size of Bank	Address Range of Segments	Size of Segments
4 Mbit	9 Row x 9 Column	1 Mbyte	n000.0000-n00F.FFFF	1 Mbyte
16 Mbit	10 Row x 10 Column	4 Mbytes	n000.0000-n03F.FFFF	4 Mbytes
16 Mbit	12 Row x 8 Column	4 Mbytes	n000.0000-n007.FFFF n010.0000-n017.FFFF n040.0000-n047.FFFF n050.0000-n057.FFFF n100.0000-n107.FFFF n110.0000-n117.FFFF n140.0000-n147-FFFF n150.0000-n157.FFFF	512 KBYTES 512 KBYTES 512 KBYTES 512 KBYTES 512 KBYTES 512 KBYTES 512 KBYTES 512 KBYTES
64 Mbit	11 Row x 11 Column	16 Mbytes	n000.0000-n0FF.FFFF	16 Mbytes

Size	Address Configuration	Total Size of Bank	Address Range of Segments	Size of Segments
64 Mbit	13 Row x 9 Column	16 Mbytes	n000.0000-n01F.FFFF n040.0000-n05F.FFFF n100.0000-n11F.FFFF n140.0000-n15F.FFFF n400.0000-n41F.FFFF n440.0000-n45F.FFFF n500.0000-n51F.FFFF n540.0000-n55F.FFFF	2Mbytes 2Mbytes 2Mbytes 2Mbytes 2Mbytes 2Mbytes 2Mbytes 2Mbytes
256 Mbit	12 Row x 12 Column	64 Mbytes	n000.0000-n3FF.FFFF	64 Mbytes
1Gbit	13 Row x 13 Column	256 Mbytes	n000.0000-nFFF.FFFF	256 MBytes

TABLE 8

Size	Address Configuration	Total Size of Bank	Address Range of Segments(s)	Size of Segment(s)
4 Mbit	9 Row x 9 Column	0.5 Mbyte	n000.0000-n007.FFFF	0.5 MByte
16 Mbit	10 Row x 10 Column	2 Mbytes	n000.0000-n01F.FFFF	2 Mbytes

Size	Address Configuration	Total Size of Bank	Address Range of Segments(s)	Size of Segment(s)
16 Mbit	12 Row x 8 Column	2 Mbytes	n000.0000-n003.FFFF n008.0000-n00B.FFFF n020.0000-n023.FFFF n028.0000-n02B.FFFF n080.0000-n083.FFFF n088.0000-n08B.FFFF n0A0.0000-n0A3.FFFF n0A8.0000-n0AB.FFFF	256 KBytes 256 KBytes 256 KBytes 256 KBytes 256 KBytes 256 KBytes 256 KBytes 256 KBytes
64 Mbit	11 Row x 11 Column	8 Mbytes	n000.000-n07F.FFFF	8 Mbytes
64 Mbit	13 Row x 9 Column	8 Mbytes	n000.0000-n00F.FFFF n020.0000-n02F.FFFF n080.0000-n08F.FFFF n0A0.0000-n0AF.FFFF n200.0000-n20F.FFFF n220.0000-n22F.FFFF n280.0000-n28F.FFFF n2A0.0000-n2AF.FFFF	1 MByte 1 MByte 1 MByte 1 MByte 1 MByte 1 MByte 1 MByte 1 MByte
256 Mbit	12 Row x 12 Column	32 Mbytes	n000.0000-n1FF.FFFF	32 Mbytes
1 Gbit	13 Row x 13 Column	128 Mbytes	n000.0000-n7FF.FFFF	128 Mbytes

TABLE 9

Address (W/B)	**Operating**	**Idle**	**Standby**	**NPOR RESET**	**NRESET RESET**
DRAM Control	On	On	SELFREF	Off	SELFREF
UARTs	On	On	Off	Reset	Reset
LCD FIFO	On	On	Reset	Reset	Reset
LCD	On	On	Off	Reset	Reset
ADC Interface	On	On	Off	Reset	Reset
SS12 Interface	On	On	Off	Reset	Reset
DAI Interface	On	On	Off	Reset	Reset
Codec	On	On	Off	Reset	Reset
Timers	On	On	Off	Reset	Reset
RTC	On	On	On	On	On
LED Flasher	On	On	On	Reset	Reset
DC-to-DC	On	On	Off	Reset	Reset
CPU	On	Off	Off	Reset	Reset
Interrupt Control	On	On	On	Reset	Reset
PLL/CLKEN Signal	On	On	Off	Off	Off

TABLE 10

Pin No. LQFP	External Pin Name	SSI2 Slave Mode (Internal Name)	SSI2 Master Mode	Codec Internal Name	DAI	Strength
63	SSICCLK	SSICCLK= serial bit clock; Input	Output	PCMCLK = Output	SCLK = Output	1
65	SSITXFR	SSKTXFR=TX frame sync; Input	Output	PCMSYNC = Output	LRCK = Output	1
66	SSITXDA	SSITXDA=TX data; Output	Output	PCMOUT = Output	SDOUT = Output	1
67	SSIRXDA	SSIRXDA=RX data; Input	Input	PCMIN = Input	SDIN = Input	
68	SSIRXFR	SSIRXFR=RX frame sync; Input	Output	p/u*	MCLK	1

*p/u = use an 10 k pull-up

TABLE 11

Type	**Comments**	**Referred To As**	**Max. Transfer Speed**
SP/Microwire 1	Master mode only	ADC Interface	128 Kbps
SPI/Microwire 2	Master/slave mode	SSI2 Interface	512 Kbps
MCP Interface	CD quality DACs and ADCs	DAI	1.536 Mbps
Codec Interface	**Only** for use in the PLL clock mode	Codec Interface	64 Kpbs

TABLE 12

SYSCON1 Bit 17	SYSCON1 Bit 16	13.0 MHz Operation ADCCLK Frequency (kHz)	18. 432-73.728 MHz Operation ADCCLK Frequency (kHz)
0	0	4.2	4
0	1	16.9	16
1	0	67.7	64
1	1	135.4	128

TABLE 13

Address (W/B)	Data In Memory	Byte Lanes to Memory/Ports/Registers								RO Contents	
		Big Endian Memory				Little Endian Memory					
		7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24	Big Endian	Little Endian
Word +0 (W)	11223344	44	33	22	11	44	33	22	11	11223344	11223344
Word +1 (W)	11223344	44	33	22	11	44	33	22	11	44112233	44112233
Word +2 (W)	11223344	44	33	22	11	44	33	22	11	33441122	33441122
Word + 3 (W)	11223344	44	33	22	11	44	33	22	11	22334411	22334411
Word +0 (B)	11223344	dc	dc	dc	11	44	dc	dc	dc	00000011	00000044
Word +1 (B)	11223344	dc	dc	22	dc	dc	33	dc	dc	00000022	00000033
Word +2 (B)	11223344	dc	33	dc	dc	dc	dc	22	dc	00000033	00000022
Word +3 (B)	11223344	44	dc	dc	dc	dc	dc	dc	11	00000044	00000011

TABLE 14

Address (W/B)	Register Contents	Byte Lanes to Memory/Ports/Registers							
		Big Endian Memory				Little Endian Memory			
		7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24
Word +0 (W)	11223344	44	33	22	11	44	33	22	11
Word +1 (W)	11223344	44	33	22	11	44	33	22	11
Word +2 (W)	11223344	44	33	22	11	44	33	22	11
Word +3 (W)	11223344	44	33	22	11	44	33	22	11
Word + 0 (B)	1223344	44	44	44	44	44	44	44	44
Word +1 (B)	11223344	44	44	44	44	44	44	44	44
Word +2 (B)	11223344	44	44	44	44	44	44	44	44
Word +3 (B)	11223344	44	44	44	44	44	44	44	44

TABLE 15

Name	Bits	Address	Comment
UNIQID	31:0	0x2440	32 bit ID
UNIQCHK	39:32	0x2450	8 bit hamming code for UNIQID
UNIQID2	159:128	0x2700	32 bit ID #2
UNIQID3	191:160	0x2704	32 bit ID #3
UNIQID4	223:192	0x2708	32 bit ID #4
UNIQID5	255:224	0x270C	Hamming codes and flags
UNIQCHK2	231:224		8 bit hamming code for UNIQID2
UNIQCHK3	239:232		8 bit hamming code for UNIQID3
UNIQCHK4	247:240		8 bit hamming code for UNIQID4
ASECEX	248		Alternate security exists
	255:249		Reserved `0'

TABLE 16

Name	Comment
PRIVID	PRIVATE ID number
PRIVHAM	PRIVATE hamming code for private ID numbers
PRIVFLG	Private firmware exists

TABLE 17

Bit	Definition
0	Good Validation
1	ID all 0's
2	CHK all 0's
3	ID all 1's
4	CHK all 1's

TABLE 18

Name	Address	ID-CHK pair
UNIQVAL	0x2460	UNIQID-UNIQCHK
UNIQVAL2	0x2720	UNIQID2-UNIQCHK2
UNIQVAL3	0x2724	UNIQID3-UNIQCHK3
UNIQVAL4	0x2728	UNIQID4-UNIQCHK4

TABLE 19

Name	Address	ID-CHK pair
SECVAL1	0x2540	SECID1-SECCHK1
SECVAL2	0x2544	SECID2-SECCHK2

TABLE 20

Name	Address	Comment
TESTID	0x27AC	32 bit general register
TESTCHK	0x2753	8 bit general register
TESTVAL	0x2744	Validation for TESTID-TESTCHK pair